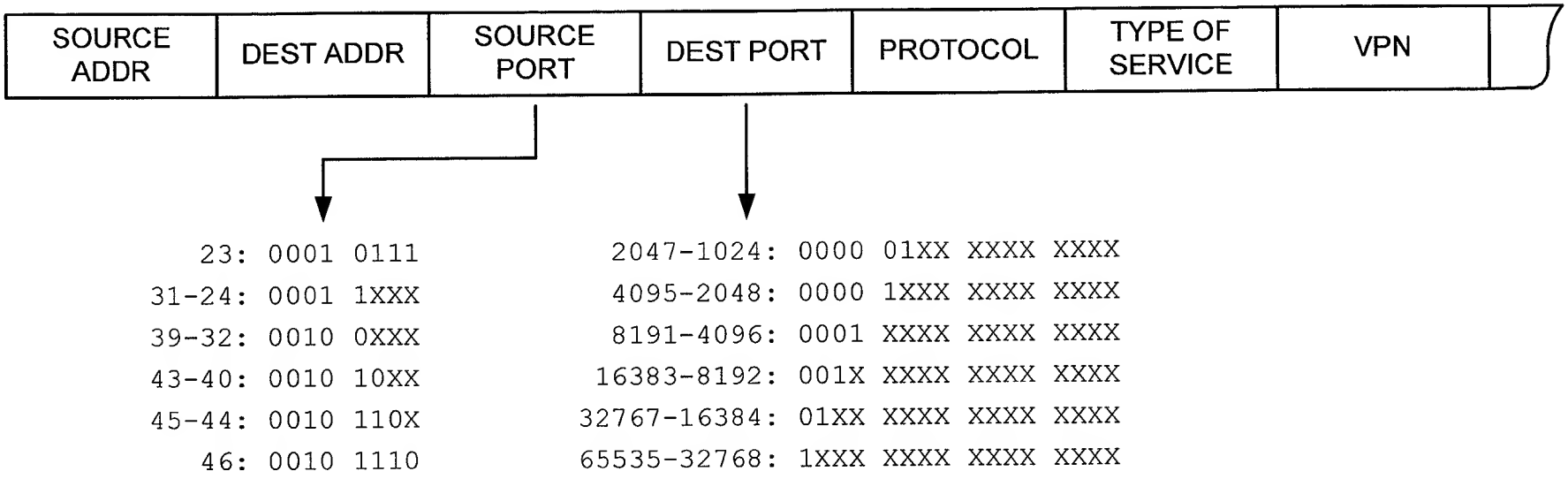


FIG. 1
(PRIOR ART)

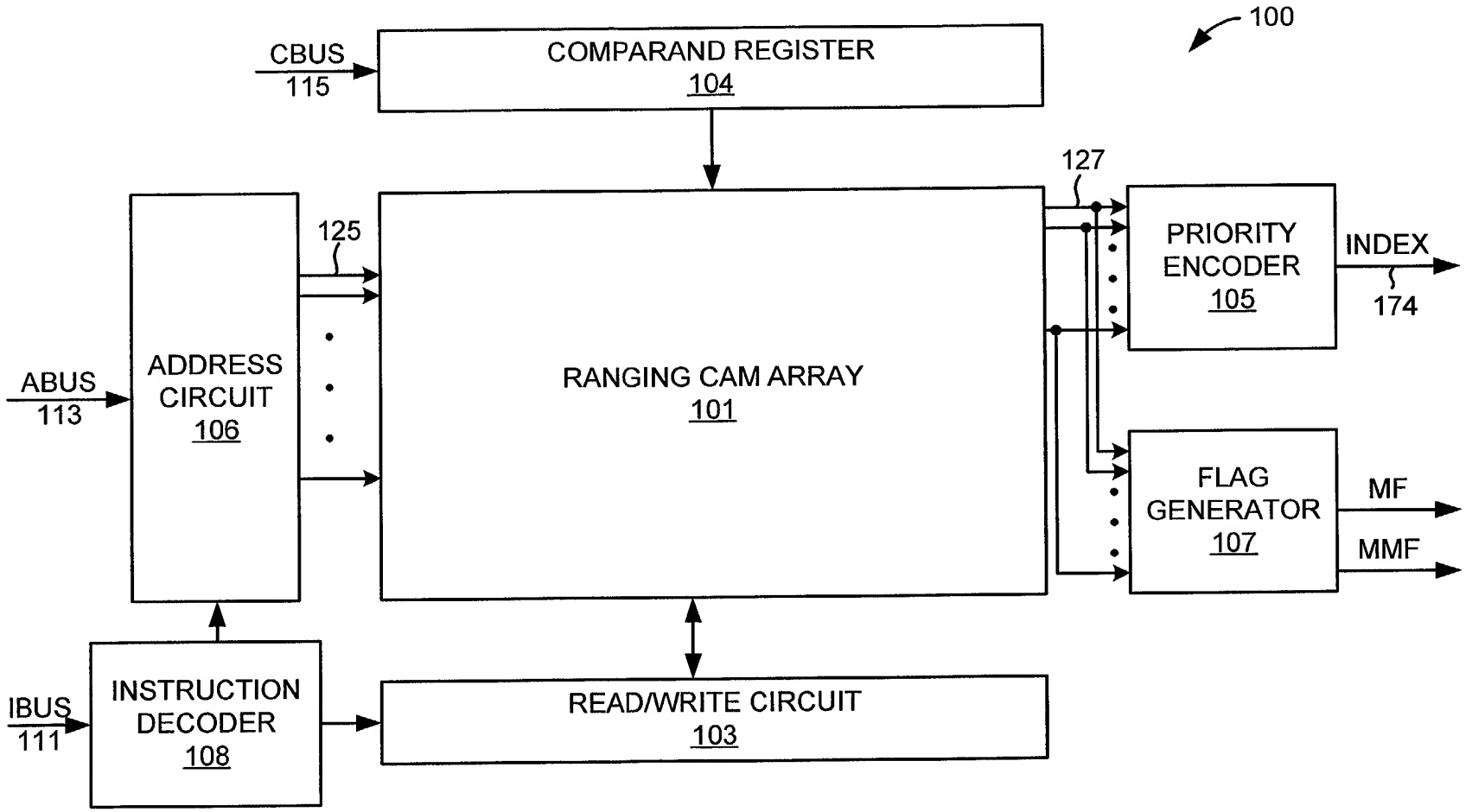

100
CBUS
115
COMPARAND REGISTER
104
127
125
PRIORITY
ENCODER
105
INDEX
174
ABUS
113
ADDRESS
CIRCUIT
106
RANGING CAM ARRAY
101
FLAG
GENERATOR
107
MF
MMF
IBUS
111
INSTRUCTION
DECODER
108
READ/WRITE CIRCUIT
103

FIG. 2

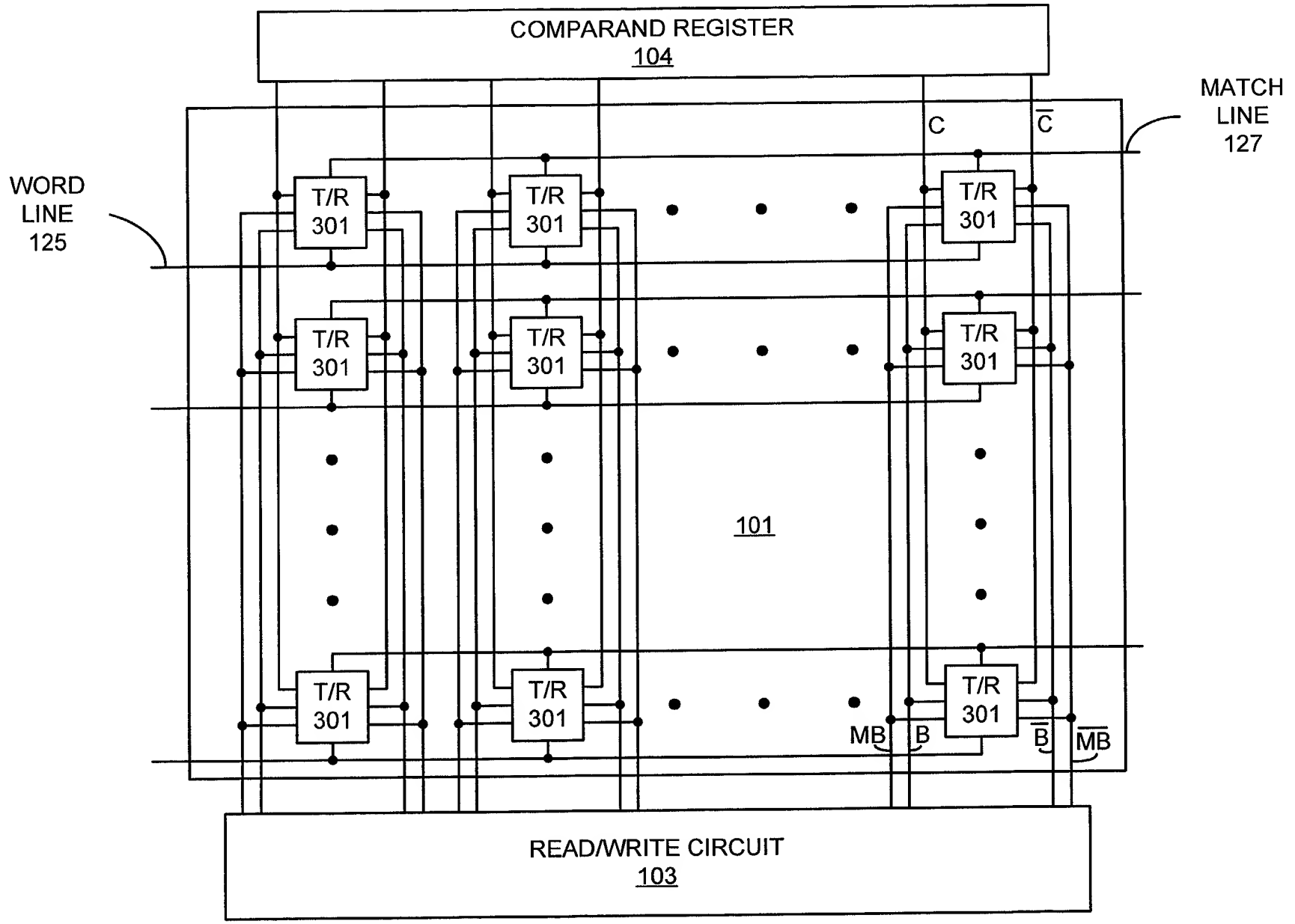

COMPARAND REGISTER
104
MATCH
LINE
127
C
$\overline{C}$
WORD
LINE
125
T/R
301
101
MB
B
$\overline{B}$
$\overline{MB}$
READ/WRITE CIRCUIT
103

FIG. 3

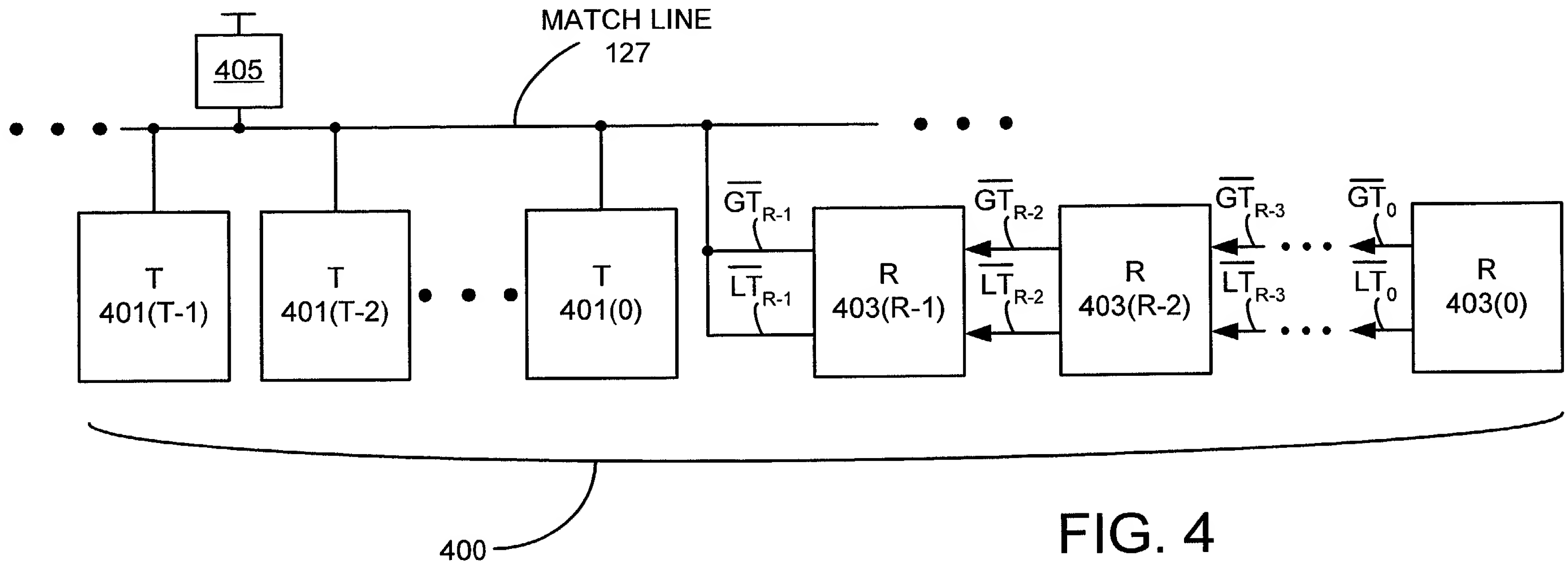

MATCH LINE
127
405
T
401(T-1)
T
401(T-2)
T
401(0)
R
403(R-1)
R
403(R-2)
R
403(0)
$\overline{GT}_{R-1}$
$\overline{LT}_{R-1}$
$\overline{GT}_{R-2}$
$\overline{LT}_{R-2}$
$\overline{GT}_{R-3}$
$\overline{LT}_{R-3}$
$\overline{GT}_{0}$
$\overline{LT}_{0}$
400

FIG. 4

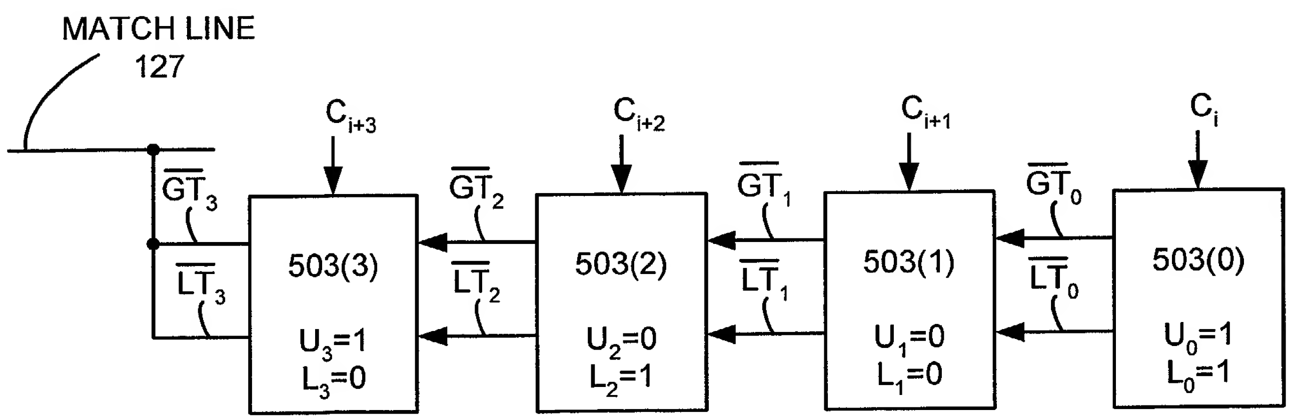

MATCH LINE
127
C_{i+3}
C_{i+2}
C_{i+1}
C_{i}
$\overline{GT}_{3}$
$\overline{LT}_{3}$
$\overline{GT}_{2}$
$\overline{LT}_{2}$
$\overline{GT}_{1}$
$\overline{LT}_{1}$
$\overline{GT}_{0}$
$\overline{LT}_{0}$
503(3)
$U_3=1$
$L_3=0$
503(2)
$U_2=0$
$L_2=1$
503(1)
$U_1=0$
$L_1=0$
503(0)
$U_0=1$
$L_0=1$

FIG. 5

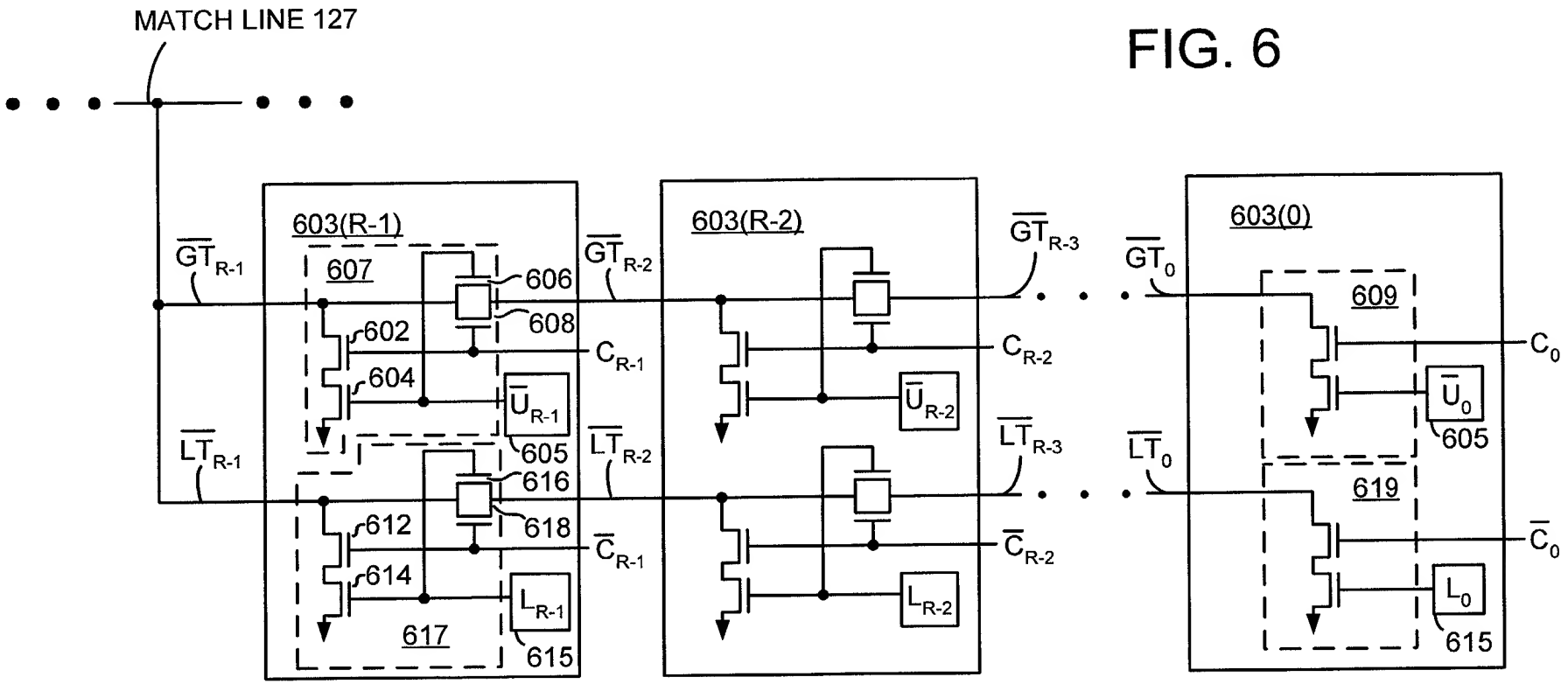


FIG. 6

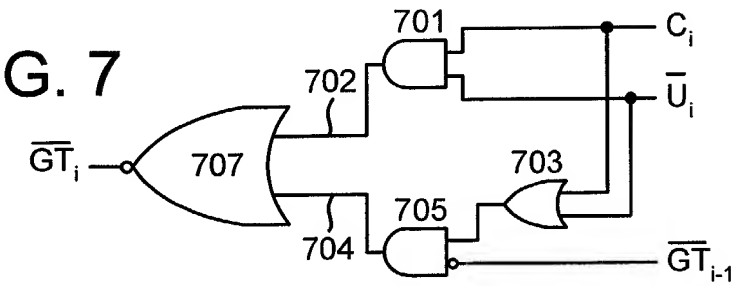


FIG. 7

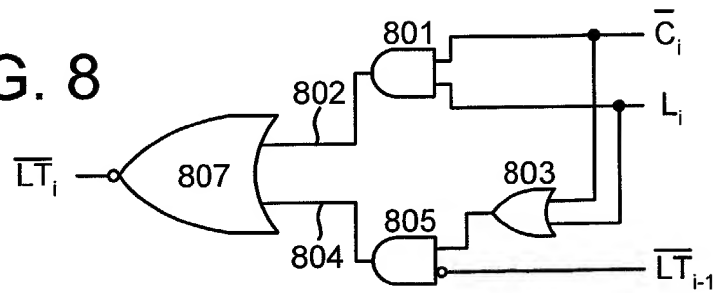


FIG. 8

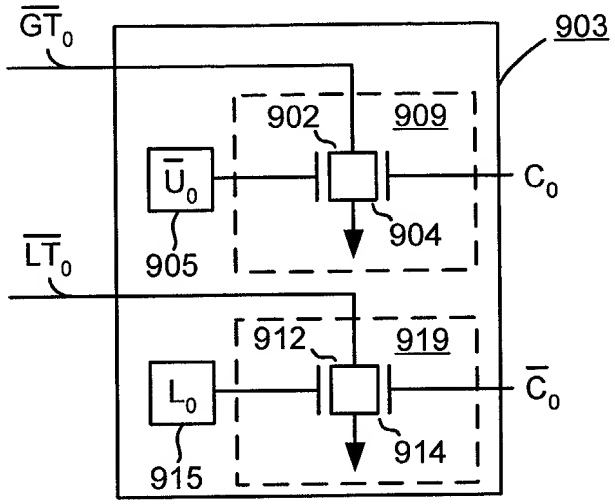

$\overline{GT}_0$
903
902
909
$\overline{U}_0$
C_0
904
905
$\overline{LT}_0$
912
919
L_0
$\overline{C}_0$
914
915

FIG. 9

FIG. 10

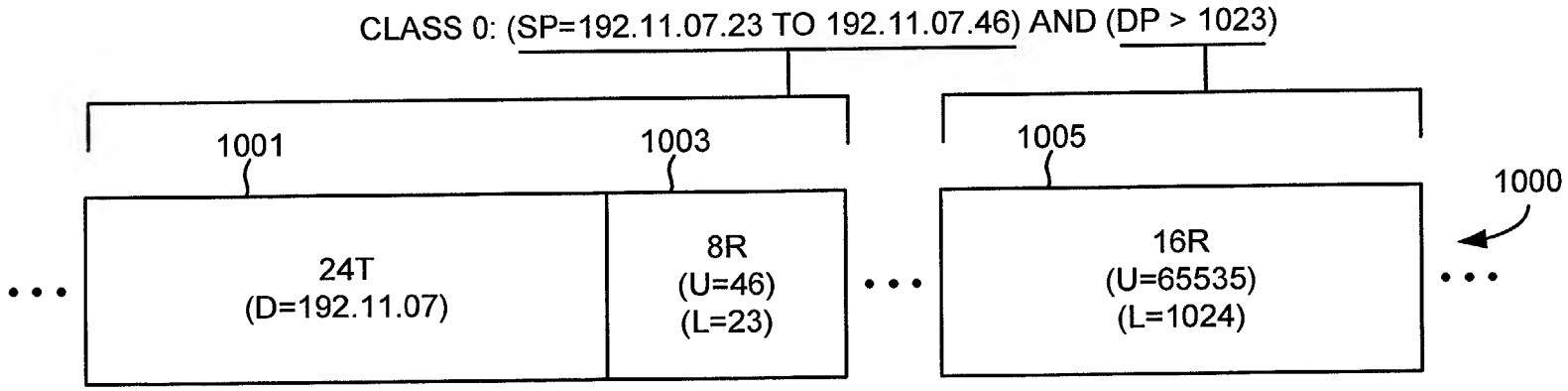
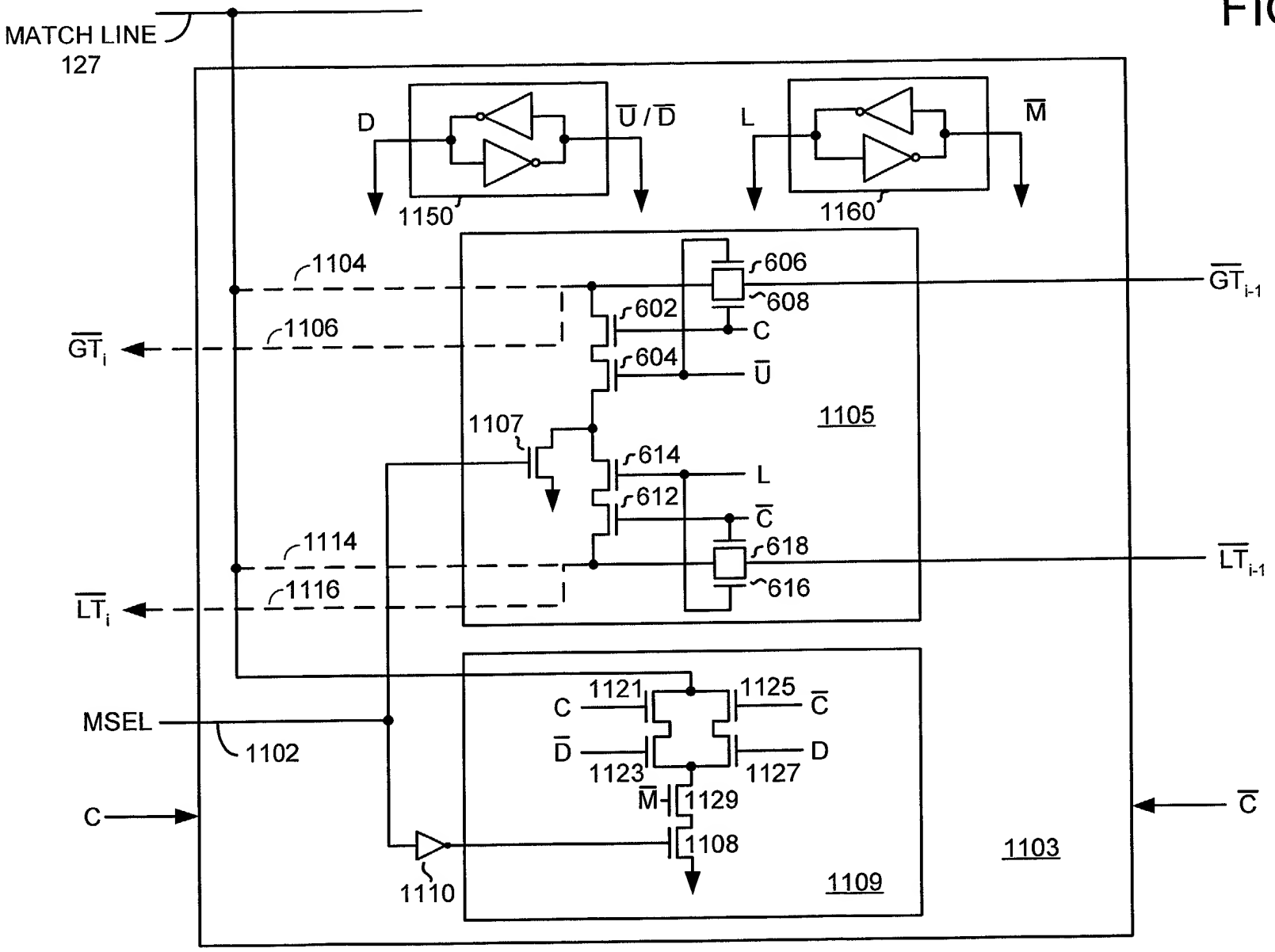

CLASS 0: (SP=192.11.07.23 TO 192.11.07.46) AND (DP > 1023)
1001
1003
1005
1000
24T
(D=192.11.07)
8R
(U=46)
(L=23)
16R
(U=65535)
(L=1024)

FIG. 11


MATCH LINE
127
D
U / D
1150
L
M
1160
1104
606
608
602
C
604
U
1105
1107
614
L
612
C
618
616
1106
1114
1116
GT_i
LT_i
GT_i-1
LT_i-1
MSEL
1102
C
1121
1125
C
D
1123
1127
D
M
1129
1108
1110
1109
1103
C

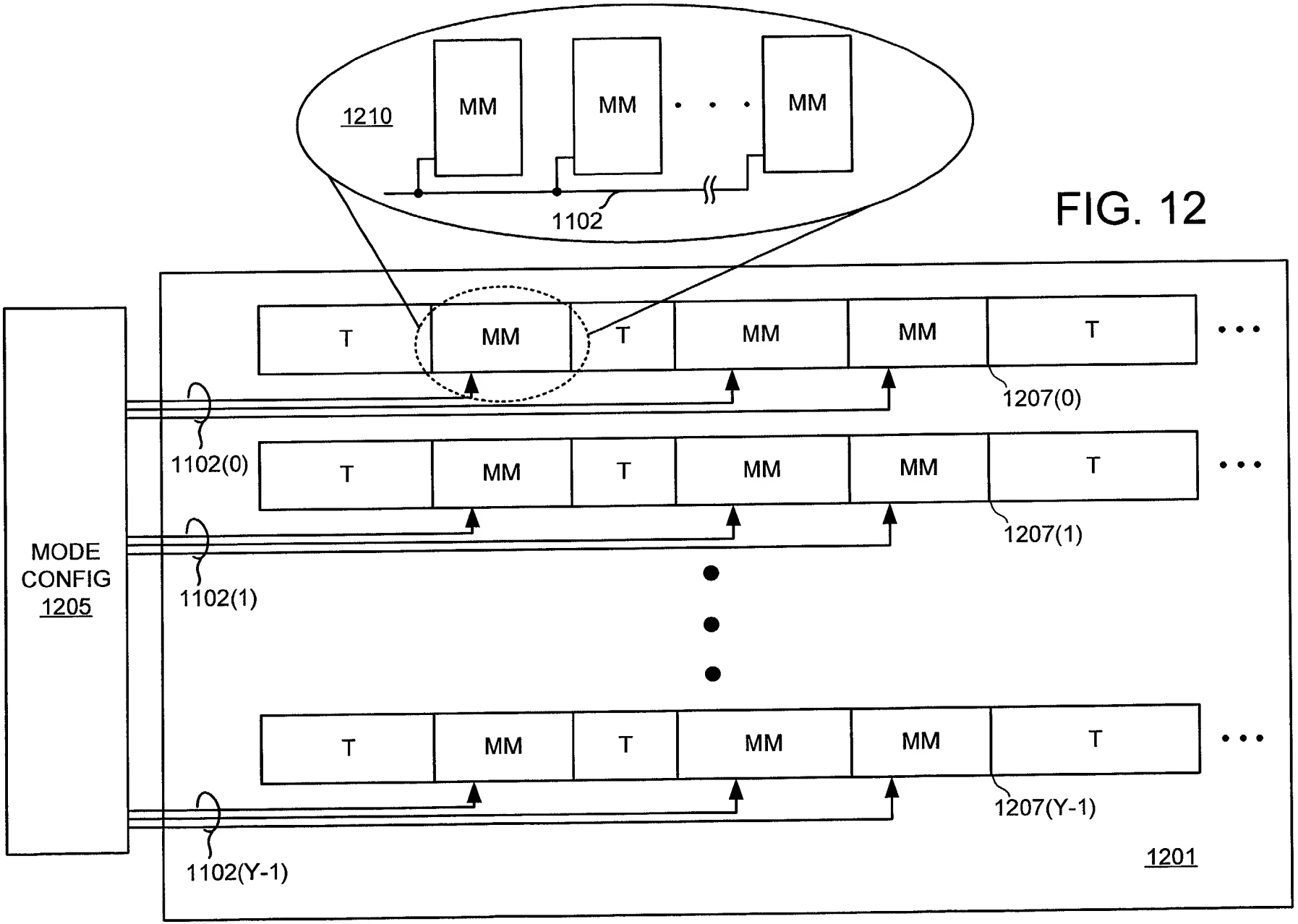


FIG. 12

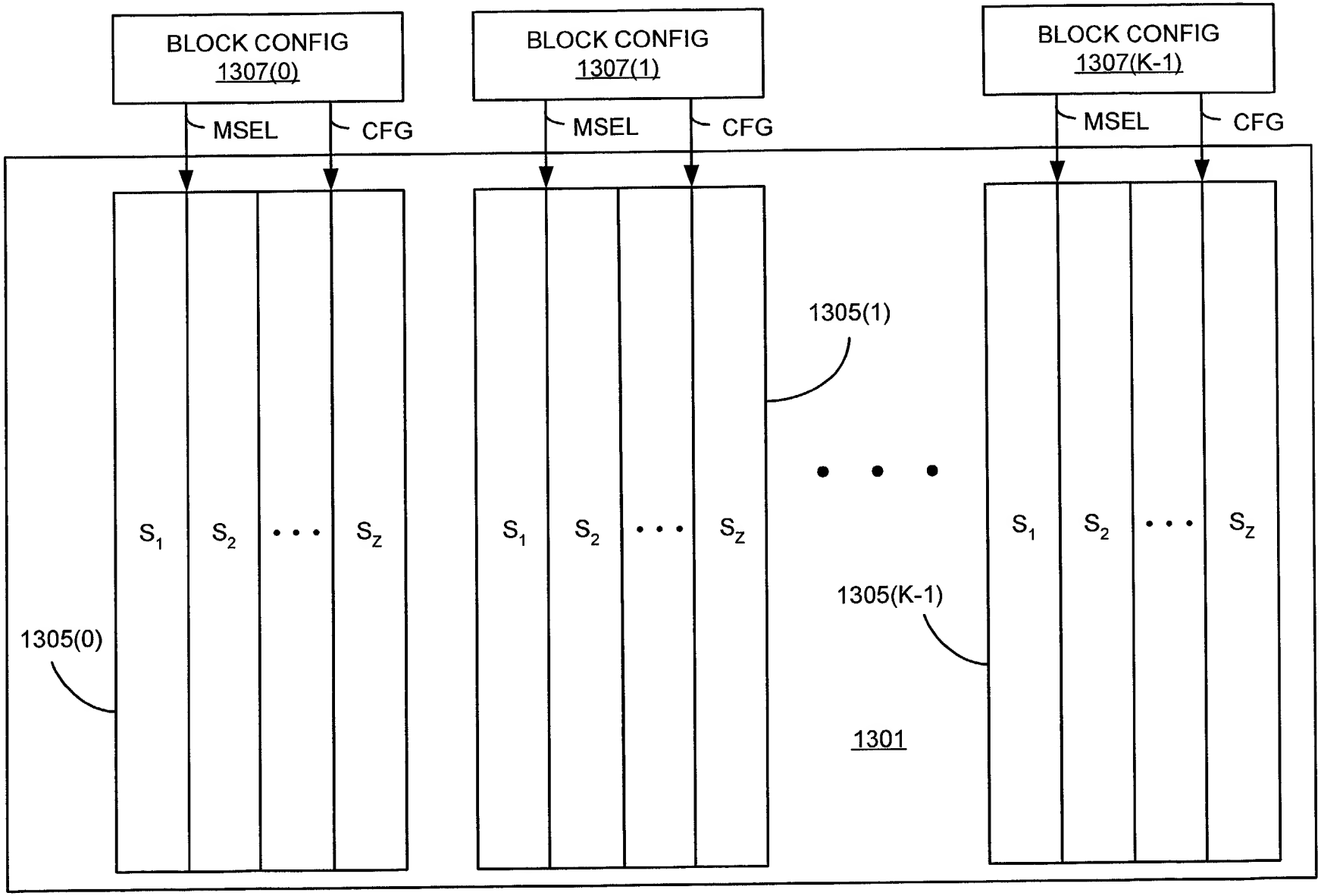
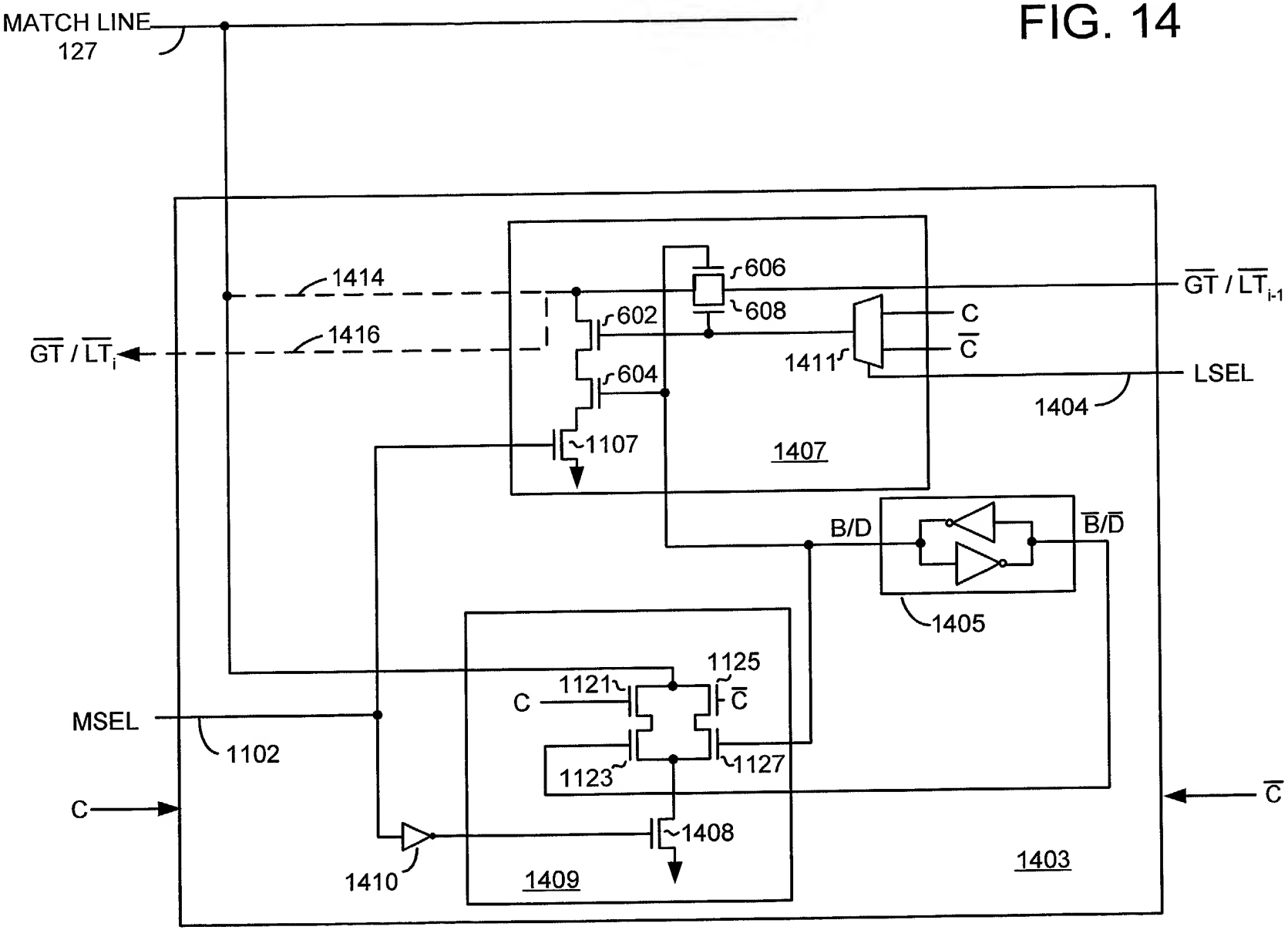

BLOCK CONFIG
1307(0)
MSEL
CFG
BLOCK CONFIG
1307(1)
MSEL
CFG
BLOCK CONFIG
1307(K-1)
MSEL
CFG
1305(1)
S1
S2
S3
SZ
1305(0)
1305(K-1)
1301

FIG. 13

FIG. 14



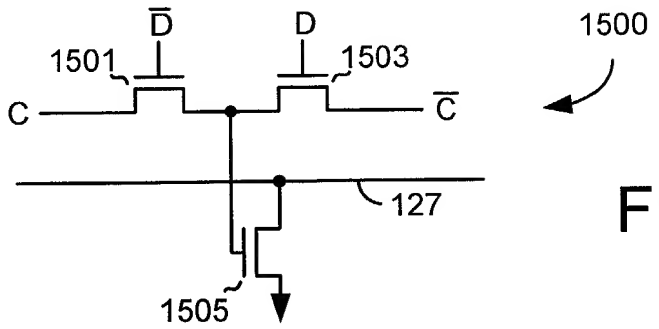

1500
$\overline{D}$
D
1501
1503
C
$\overline{C}$
127
1505

FIG. 15

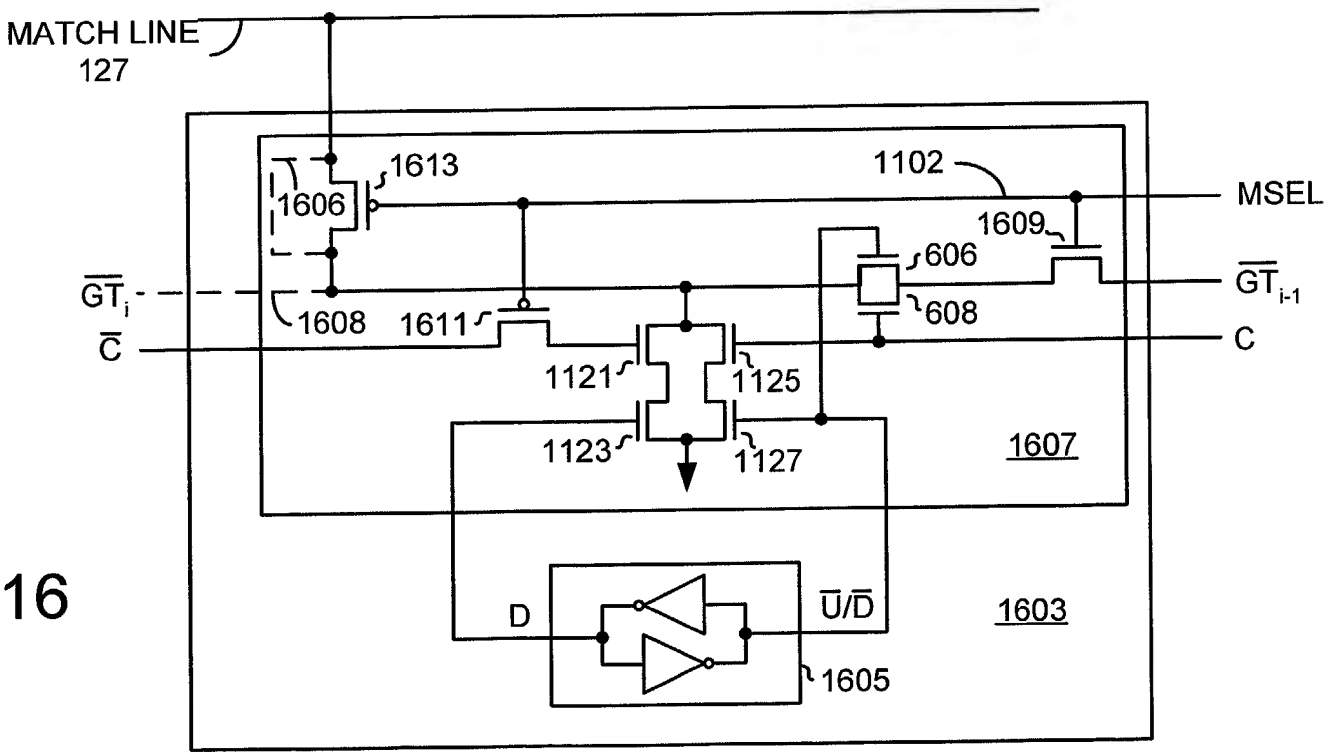

MATCH LINE
127
1613
1606
1102
MSEL
1609
606
$\overline{GT}_i$
$\overline{GT}_{i-1}$
608
1608
1611
$\overline{C}$
C
1121
1125
1123
1127
1607
D
$\overline{U}/\overline{D}$
1603
1605

FIG. 16

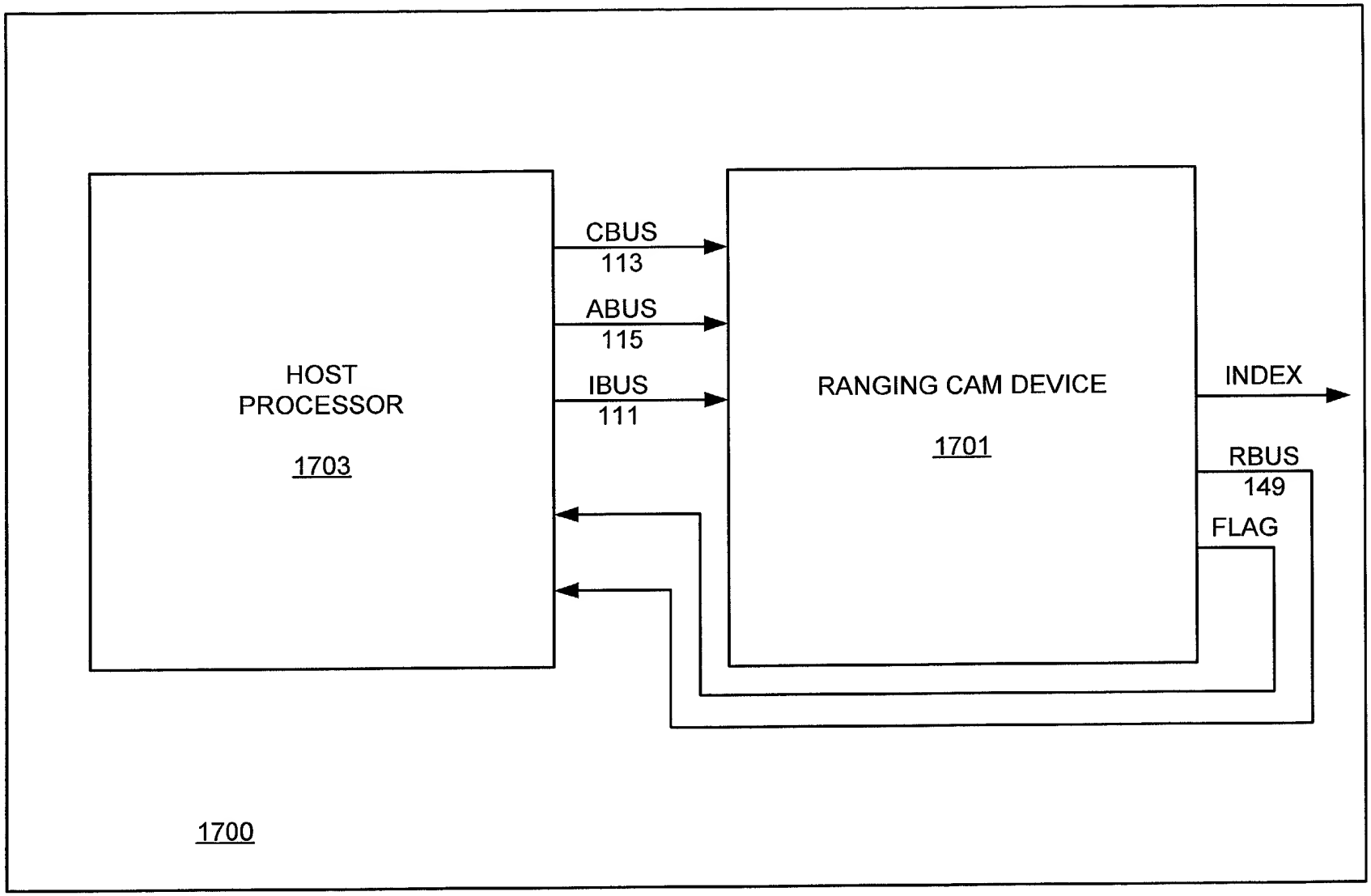

HOST
PROCESSOR
1703
CBUS
113
ABUS
115
IBUS
111
RANGING CAM DEVICE
1701
INDEX
RBUS
149
FLAG
1700

FIG. 17

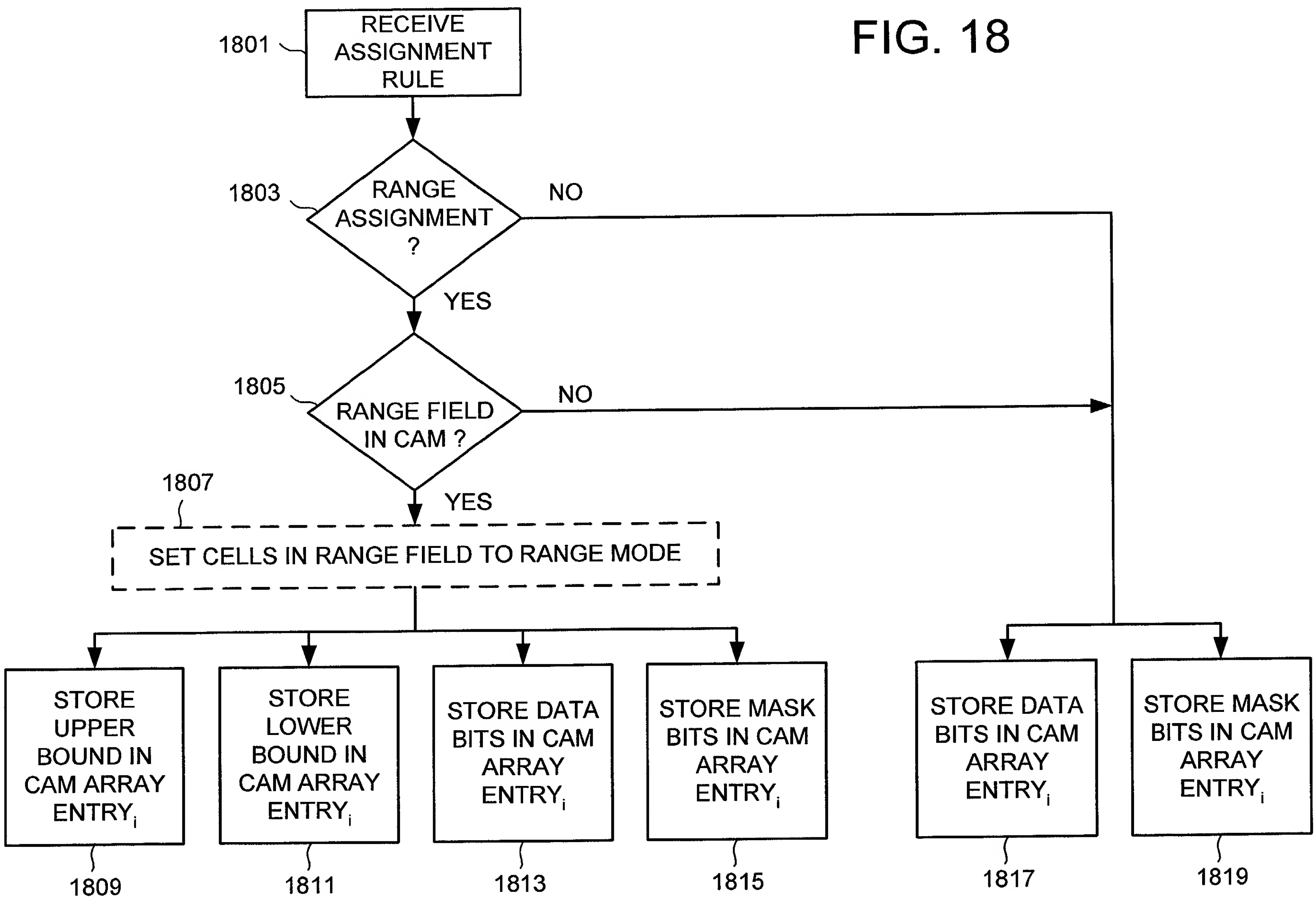

RECEIVE ASSIGNMENT RULE
1801
RANGE ASSIGNMENT ?
1803
NO
YES
RANGE FIELD IN CAM ?
1805
NO
YES
SET CELLS IN RANGE FIELD TO RANGE MODE
1807
STORE UPPER BOUND IN CAM ARRAY ENTRY$_i$
1809
STORE LOWER BOUND IN CAM ARRAY ENTRY$_i$
1811
STORE DATA BITS IN CAM ARRAY ENTRY$_i$
1813
STORE MASK BITS IN CAM ARRAY ENTRY$_i$
1815
STORE DATA BITS IN CAM ARRAY ENTRY$_i$
1817
STORE MASK BITS IN CAM ARRAY ENTRY$_i$
1819

FIG. 18